



GODAVARI INSTITUTE OF ENGINEERING & TECHNOLOGY GRMT-20

Autonomous
NBA Accredited & NAAC A+

Approved by AICTE, Accredited by NAAC 'A+' Grade, Recognized under 2(f) and 12(b) of UGC, Permanently Affiliated to JNTUK, Kakinada.

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

M.Tech - VLSI & Embedded Systems Course Structure and Syllabus: (2020-21)

COURSE STRUCTURE & SYLLABUS for M. Tech

VLSI & ES

(Applicable for batches admitted from 2020 - 21)



Godavari institute of Engg & Technology

Approved By AICTE NAAC 'A+' Grade Recognized by UGC, U/Sec.2(f)&12(B) Permanent affiliation by JNTUK

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
M.Tech - VLSI & Embedded Systems Course Structure and Syllabus: (2020-21)
I YEAR I SEMESTER
W.E.F Academic year 2020-21

Sl. No.	Course Code	Course Category	Subject Title	Periods per week			C	Scheme of Examination Maximum Marks		
				L	T	P		Int.	Ext.	Total
1		PCC	RTL Simulation and Synthesis with PLDs	3	0	0	3	40	60	100
2		PCC	Microcontrollers Programmable Digital Signal Processors	3	0	0	3	40	60	100
3		PEC	Professional Elective – I a. VLSI Technology and Design b. VLSI Signal Processing c. CAD of Digital System	3	0	0	3	40	60	100
4		PEC	Professional Elective – II a. Programming Languages for Embedded Systems b. Advanced Computer Architecture c. Embedded System Design	3	0	0	3	40	60	100
5		MC	Research Methodology	2	0	0	2	40	60	100
6		AC	Audit Course -1	2	0	0	0	40*	-	-
7		PCC	RTL Simulation and Synthesis with PLDs Lab	0	0	4	2	50	50	100
8		PCC	Microcontrollers and Programmable Digital Signal Processors Lab	0	0	4	2	50	50	100
TOTAL				16	0	8	18	300	400	700

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I YEAR II SEMESTER
W.E.F Academic year 2020-21

Sl. No.	Course Code	Course Category	Subject Title	Periods per week			C	Scheme of Examination Maximum Marks		
				L	T	P		Int.	Ext.	Total
1		PCC	Analog & Digital CMOS VLSI Design	3	0	0	3	40	60	100
2		PCC	Real Time Operating Systems	3	0	0	3	40	60	100
3		PEC	Professional Elective – III	3	0	0	3	40	60	100
			a. System Design with Embedded Linux							
			b. Communication Buses & Interfaces							
		PEC	Professional Elective – IV	3	0	0	3	40	60	100
		a. Physical Design Automation								
		b. SoC Design								
		PEC	c. Low Power VLSI Design							
5		AC	Audit Course – 2	2	0	0	0	40*	-	-
6		PCC	Analog & Digital CMOS VLSI Design Lab	0	0	4	2	50	50	100
7		PCC	Real Time Operating Systems Lab	0	0	4	2	50	50	100
8		ESC	Mini Project	0	0	4	2	100	-	100
TOTAL				14	0	12	18	360	340	700

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II YEAR I SEMESTER
W.E.F Academic year 2020-21

Sl. No.	Course Code	Course Category	Subject Title	Periods per week			C	Scheme of Examination Maximum Marks		
				L	T	P		Int.	Ext.	Total
1		PEC / MOOCS*	Professional Elective – V a. IOT and its Applications b. Design for Testability c. Artificial Intelligence	3	0	0	3	40	60	100
2		OEC / MOOCS*	a. Composite Materials b. Cost Management of Engineering Projects c. Machine Learning d. Cyber Security e. Energy Audit Conservation and Management f. Utilization of Electrical Energy g. Operations Research h. Nano Technology	3	0	0	3	40	60	100
3		PR	Dissertation – I/Industrial Project <i>(to be continued and evaluated next sem)</i>	0	0	20	10	-	-	-
TOTAL				6	0	20	16	80	120	200

*Students going for Industrial Project/Thesis will complete these courses through MOOCs.

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II YEAR II SEMESTER
W.E.F Academic year 2020-21

Sl. No.	Course Code	Course Category	Subject Title	Periods per week			C	Scheme of Examination Maximum Marks		
				L	T	P		Int.	Ext.	Total
1		PR	Project/Dissertation – II	0	0	32	16	-	-	-

Audit Course 1&2:

1. English for Research Paper Writing
2. Disaster Management
3. Value Education
4. Constitution of India

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M.Tech - VLSI & Embedded Systems Course Structure and Syllabus: (2020-21)
I YEAR I SEMESTER

Regulation GRMT-20	Godavari Institute of Engineering & Technology (Autonomous)	I M.Tech. I Sem (1 st Semester)			
Course Code	RTL SIMULATION AND SYNTHESIS WITH PLDs				
Teaching	Total contact hours-45	L	T	P	C
Prerequisites: Knowledge of Digital Electronics and Digital IC Design.		3	-	-	3

Course Objectives:

1. To introduce Verilog HDL for the design and functionality verification of a digital circuit.
3. To understand the design of data path and control circuits for sequential machines.
4. To introduce the concept of realizing a digital circuit using PLDs.
5. To learn the issues in ASIC prototyping using FPGAs.
6. To understand design challenges and how to overcome practical issues and concerns.

Course Outcomes:

On completion of the course, the students will be able to	
CO1:	Develop the Verilog HDL code to design a digital circuit.
CO2:	Appreciate the analysis of finite state machine of a controlling circuit.
CO3:	Develop finite state machines and RTL design using reconfigurable logic.
CO4:	Understand the static timing analysis and clock issues in digital circuits.
CO5:	Verify the functionality of the digital designs using PLDs.

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING**M.Tech - VLSI & Embedded Systems Course Structure and Syllabus: (2020-21)****UNIT – 1 Verilog HDL**

Importance of HDLs, Lexical Conventions of Verilog HDL, Gate level modeling: Built in primitive gates, Switches, Gate delays. Data flow modeling: Continuous and implicit continuous assignment, Delays. Behavioral modeling: Procedural constructs, Control and repetition statements, Delays, Function and Tasks.

UNIT – 2 Digital Design

Design of BCD Adder, State graphs for control circuits, Shift and add multiplier, Binary divider. FSM and SM Charts: Finite state diagram, Implementation of sequence detector using FSM, State machine charts, Derivation of SM Charts, Realization of SM Chart, Implementation of Binary Multiplier.

UNIT – 3 ASIC Design Flow

Simulation, Simulation types, Synthesis, Synthesis methodologies, Translation, Mapping, Optimization, Floor planning, Placement, Routing, Clock tree synthesis, Physical verification.

UNIT – 4 Static Timing Analysis

Timing paths, Meta-stability, Clock issues, Need and design strategies for multi-clock domain designs, Setup and hold time violations, Steps to remove setup and hold time violations.

UNIT – 5 Digital Design using PLDs

ROM, PLA, PAL-Registered PALs, Configurable PALs, GAL.CPLDs: Features, Programming and applications using complex programmable logic devices. FPGAs: Field Programmable gate arrays, Logic blocks, Routing architecture, Design flow.

Text Books:

1. Verilog HDL-A Guide to Digital Design and Synthesis, Samir Palnitkar, 2nd Edition, 2003.
2. Fundamentals of Logic Design, Charles H. Roth, 5th Edition, Cengage Learning, 2010.
3. Verilog HDL Synthesis - A Practical Primer, Bhasker J, 1st edition, 1998.

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Reference Books:

1. Digital principles and Design, Donald D Givone, TMH, 2016.
2. Designing with FPGAs & CPLDs, Bob Zeidman, CMP Books, 2002.
3. Modern Digital Design, Richard S. Sandige, MGH, International Editions, 1990.

Web Links:

1. <https://nptel.ac.in/courses/106/103/106103206/>
2. https://swayam.gov.in/nd1_noc19_cs62/preview
3. <http://course.ece.cmu.edu/~ece447/s13/lib/exe/fetch.php?media=onur-447-spring13-lecture33-heterogeneousmulticore-afterlecture.pdf>
4. <https://www.ee.iitb.ac.in/~viren/Courses/2015/CS683.htm>

CO-PO Mapping:
1: Slight (Low) 2: Moderate (Medium) 3: Substantial (High) '-': No Correlation

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	2	1	3	-	1	1	1	-	-	-	1	3
CO2	2	1	1	-	-	-	1	2	-	2	-	-
CO3	2	-	3	2	1	2	2	-	3	-	2	-
CO4	1	2	-	-	-	2	3	3	2	1	-	3
CO5	3	-	-	2	-	1	-	2	-	2	-	-

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Regulation GRMT-20	Godavari Institute of Engineering & Technology (Autonomous)	I M.Tech. I Sem (1 st Semester)			
Course Code	MICROCONTROLLERS AND PROGRAMMABLE DIGITAL SIGNAL PROCESSORS				
Teaching	Total Contact Hours-45	L	T	P	C
Prerequisites: Knowledge of Computer Architecture and Organization, Microcontrollers and C programming.		3	-	-	3

Course Objectives:

1. To understand, compare and select ARM processor core based SoC with several features/peripherals based on requirements of embedded applications.
2. To understand several memory interfacing and accessing methods.
3. To identify and characterize architecture of Programmable DSP Processors.
4. To develop various on-chip and off-chip devices interfacing concepts.
5. To develop small applications by utilizing the ARM processor core and DSP processor-based platform.

Course Outcomes:

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CO1:	Compare and select ARM processor core based SoC with several features/peripherals based on requirements of embedded applications.
CO2:	Apply RAM and ROM memory interfacing concepts and address calculations.
CO3:	Identify and characterize architecture of Programmable DSP Processors.
CO4:	Analyze the concepts of Input / Output device interfacing with processors.
CO5:	Develop small applications by utilizing the ARM processor core and DSP processor-based platform.

UNIT-1 ARM Cortex-M3 processor

Introduction, Applications, Programming model – Registers, Operation modes, Exceptions and Interrupts, Reset Sequence Instruction Set, Unified Assembler Language, Memory Maps, Memory Access Attributes, Permissions, Bit-Band Operations, Unaligned and Exclusive Transfers, Pipeline, Bus Interfaces.

UNIT – 2 Exceptions and Interrupts

Exceptions, Types, Priority, Vector Tables, Interrupt Inputs and Pending behaviour, Fault Exceptions, Supervisor and Pendable Service Call, Nested Vectored Interrupt Controller, Basic Configuration.

UNIT – 3 LPC 17xx Microcontroller

LPC 17xx microcontroller –Architecture, Internal memory, GPIOs, Timers, ADC, UART and other serial interfaces, PWM, RTC, WDT.

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING**M.Tech - VLSI & Embedded Systems Course Structure and Syllabus: (2020-21)****UNIT – 4 Programmable DSP (P-DSP) Processors**

Harvard architecture, Multi port memory, architectural structure of P-DSPMAC unit, Barrel shifters, Introduction to TI DSP processor family.

UNIT – 5 VLIW architecture and TMS320C6000

VLIW architecture and TMS320C6000 series, architecture study, data paths, cross paths, Introduction to Instruction level architecture of C6000 family, Assembly Instructions memory addressing, for arithmetic, logical operations. Code Composer Studio for application development for digital signal processing.

Text Books:

1. The definitive guide to ARM Cortex-M3, Joseph Yiu, Elsevier, 2nd Edition.
2. Digital Signal Processors: Architecture, Programming and Applications, Venkatramani B. and Bhaskar M., TMH, 2nd Edition.
3. ARM System Developer's Guide: Designing and Optimizing, Sloss Andrew N, Symes Dominic, Wright Chris, Morgan Kaufman Publication.

Reference Books:

1. ARM System-on-Chip Architecture, Steve Furber, Pearson Education.
2. Embedded System Design, Frank Vahid and Tony Givargis, Wiley.

Web Links:

1. Technical references and user manuals on www.arm.com
2. <https://www.ti.com>
3. <https://www.sanfoundry.com/arm7>
4. <https://www.sanfoundry.com/dsp>

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CO-PO Mapping:
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	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	1	1	3	-	1	1	3	2	-	1	1	3
CO2	1	2	-	1	2	-	1	2	-	3	-	-
CO3	2	-	3	2	-	2	3	-	3	1	2	-
CO4	1	2	-	1	1	2	3	3	2	1	-	3
CO5	3	-	-	2	-	1	-	2	-	2	-	-

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Regulation GRMT-20	Godavari Institute of Engineering & Technology (Autonomous)	I M.Tech. I Sem (1 st Semester)			
Course Code	VLSI TECHNOLOGY AND DESIGN (Professional Elective – I)				
Teaching	TotalContactHours-45	L	T	P	C
Pre requisites: Knowledge of Analog & Digital Electronic Circuits.		3	-	-	3

Course Objectives:

1. To learn the basic MOS Circuits.
2. To understand the MOS process technology.
3. To understand the operation of MOS devices.
4. To impart in-depth knowledge about analog and digital CMOS circuits.
5. To learn techniques of chip design using programmable devices.

Course Outcomes:

On Completion of the course, the students will be able to	
CO1:	Review FET fundamentals for VLSI design.
CO2:	Acquire knowledge about stick diagrams and layouts.
CO3:	Understand the physical design process of VLSI design flow.
CO4:	Design the subsystems based on VLSI concepts.
CO5:	Learn the design methodologies of chip design.

UNIT – 1 VLSI Technology & Design

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Fundamentals and applications, IC production process, Semiconductor processes, Design rules and Process parameters, Layout techniques and Process parameters. VLSI Design: Electronic design automation concept, ASIC and FPGA design flows, SOC designs, Design technologies: Combinational design techniques, Sequential design techniques, State machine logic design techniques and Design issues.

UNIT – 2 CMOS VLSI Design

MOS Technology and fabrication process of pMOS, nMOS, CMOS and Bi-CMOS technologies, Comparison of different processes. Building Blocks of a VLSI circuit: Computer architecture, Memory architectures, Communication interfaces, Mixed signal interfaces. VLSI Design Issues: Design process, Design for testability, Technology options, Power calculations, Package selection, Clock mechanisms, Mixed signal design.

UNIT – 3 MOS and BiCMOS Circuits

Basic electrical properties of MOS and BiCMOS circuits, MOS and BiCMOS circuit design processes, Basic circuit concepts, Scaling of MOS circuits- Qualitative and Quantitative analysis with proper illustrations and necessary derivations of expressions.

UNIT – 4 Subsystem Design

Subsystem Design and Layout: Some architectural issues, Switch logic, Gate logic, Examples of structured design (combinational logic), Some clocked sequential circuits, Other system considerations. Subsystem Design Process: Some general considerations and an illustration of design processes, Design of an ALU subsystem.

UNIT – 5 Floor Planning and Chip Design

Floor Planning: Introduction, Floor planning methods, Off-chip connections. Architecture Design: Introduction, Register-Transfer design, High-level synthesis, Architectures for low power, Architecture testing. Chip Design: Introduction and Design methodologies.

Text Books:

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1. Essentials of VLSI Circuits and Systems, K. Eshraghian, Douglas A. Pucknell, SholehEshraghian,2005, PHI Publications.
2. Modern VLSI Design-Wayne Wolf, 3rdEd., 1997, Pearson Education.
3. VLSI Design-Dr.K.V.K.K.Prasad, KattulaShyamala, Kogent Learning Solutions Inc., 2012.

Reference Books:

1. SVLSI Design Technologies for Analog and Digital Circuits, Randall L.Geiger, Phillip E.Allen, Noel R.Strader, TMH Publications, 2010.
2. Introduction to VLSI Systems: A Logic, Circuit and System Perspective- Ming-BO Lin, CRCPress, 2011.
3. Principals of CMOS VLSI Design-N.H.E Weste, K. Eshraghian, 2ndEdition, Addison Wesley.

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	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	2	-	-	-	-	-	-	-	2	-	-
CO2	3	2	-	-	2	-	-	-	-	2	-	-
CO3	3	2	-	-	-	-	-	-	-	2	-	-
CO4	3	2	-	-	2	-	-	-	-	2	-	-
CO5	3	2	-	-	-	-	-	-	-	2	-	-

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Regulation GRMT-20	Godavari Institute of Engineering & Technology (Autonomous)	I M.Tech. I Sem (I semester)			
Course Code	VLSI SIGNAL PROCESSING (Professional Elective - I)				
Teaching	Total contact hours- 45	L	T	P	C
Prerequisites: Digital circuits, Digital signal processing and Basics of VLSI		4	-	-	3

Course Objectives:

1. To understand the fundamentals of VLSI signal processing and expose them to examples of applications.
2. To develop understanding the design and optimization of VLSI architectures for basic DSP algorithms.
3. To have an advanced level knowledge on VLSI DSP Systems.

Course Outcomes:

On Completion of the course, the students will be able to	
CO1:	Understand VLSI design methodology for signal processing systems
CO2:	Be familiar with VLSI algorithms and architectures for DSP.
CO3:	Be able to implement basic architectures for DSP using CAD tools.
CO4:	Be able to get the knowledge about the various VLSI structures for signal processing.

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UNIT-I Introduction to DSP

Typical DSP algorithms, DSP algorithms benefits, Representation of DSP algorithms Pipelining and Parallel Processing Introduction, Pipelining of FIR Digital filters, Parallel Processing, Pipelining and Parallel Processing for Low Power Retiming Introduction, Definitions and Properties, Solving System of Inequalities, Retiming Techniques.

UNIT-II Folding and Unfolding

Folding- Introduction, Folding Transform, Register minimization Techniques, Register minimization in folded architectures, folding of Multirate systems Unfolding- Introduction, An Algorithm for Unfolding, Properties of Unfolding, critical Path, Unfolding and Retiming, Applications of Unfolding.

UNIT-III Systolic Architecture Design

Introduction, Systolic Array Design Methodology, FIR Systolic Arrays, Selection of Scheduling Vector, Matrix Multiplication and 2D Systolic Array Design, Systolic Design for Space Representations contain Delays.

UNIT-IV Fast Convolution

Introduction –Cook-Toom Algorithm–Winograd algorithm – Iterated Convolution – Cyclic Convolution – Design of Fast Convolution algorithm by Inspection.

UNIT-V

Digital lattice filter structures, bit level arithmetic, architecture, redundant arithmetic. Numerical strength reduction, synchronous, wave and asynchronous pipe lines, low power design. Low Power Design: Scaling Vs Power Consumption, Power Analysis, Power Reduction techniques, Power Estimation Approaches.

Text Books:

1. Keshab K. Parthi, VLSI Digital signal processing systems, design and implementation[A2], Wiley, Inter Science, 1999.
2. Mohammad Isamail and Terri Fiez, Analog VLSI signal and information processing, McGraw Hill, 1994
3. S.Y. Kung, H.J. White House, T. Kailath, VLSI and Modern Signal Processing, Prentice Hall, 1985.

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Reference Books:

1. Jose E. France, YannisTsividis, Design of Analog Digital VLSI Circuits for Telecommunications and Signal Processing' Prentice Hall, 1994.

Web Links:

1. https://swayam.gov.in/nd1_noc20_ee44/preview
2. <https://nptel.ac.in/noc/courses/noc20/SEM1/noc20-ee44/>
3. <https://www.youtube.com/watch?v=uWtsJ9KYRnE>

CO-PO Mapping:

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	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	2	-	-	-	-	-	-	-	2	-	-
CO2	3	2	-	-	-	-	-	-	-	2	-	-
CO3	3	2	-	-	-	-	-	-	-	2	-	-
CO4	3	3	-	-	-	-	-	-	-	2	-	-

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Regulation GRMT-20	Godavari Institute of Engineering & Technology (Autonomous)	I M.Tech. I Sem (1 st Semester)			
Course Code	CAD OF DIGITAL SYSTEM (Professional Elective – I)				
Teaching	Total Contact Hours-45	L	T	P	C
Prerequisites: Knowledge of VLSI Design and fabrication, VHDL/Verilog programming.		3	-	-	3

Course Objectives:

1. To understand the fundamentals of CAD tools for modeling, design, test and verification of VLSI systems.
2. To study various phases of CAD, including simulation, physical design, test and Verification.
3. To be able to demonstrate the knowledge of computational algorithms and tools for CAD.

Course Outcomes:

On Completion of the course, the students will be able to	
CO1:	Fundamentals of CAD tools for modelling, design, test and verification of VLSI systems.
CO2:	Understand various phases of CAD, including simulation, physical design, test and verification.
CO3:	Demonstrate knowledge of computational algorithms and tools for CAD.
CO4:	Understand Hardware Models for High level Synthesis.
CO5:	Perform Verilog implementation of simple circuits.

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UNIT-1 Introduction to VLSI Methodologies

Design and Fabrication of VLSI Devices, Fabrication Materials, Transistor Fundamentals, Fabrication of VLSI Circuits, Design Rules Layout of Basic Devices, Fabrication Process and its Impact on Physical Design, Scaling Methods, Status of Fabrication Process, Issues related to the Fabrication Process, Future of Fabrication Process, Solutions for Interconnect Issues, Tools for Process Development.

UNIT – 2 VLSI design automation tools

Data Structures and Basic Algorithms, Basic Terminology, Complexity Issues and NP-hardness, Basic Algorithms, Basic Data Structures, graph theory and Computational complexity, tractable and intractable problems.

UNIT – 3 General purpose methods for combinational optimization

Partitioning- Problem Formulation, Classification of Partitioning Algorithms, Group Migration Algorithms, Simulated Annealing Simulated Evolution, Other Partitioning Algorithms Performance Driven Partitioning. **Floor planning-** Chip planning, Pin Assignment, Integrated Approach. **Placement-** Problem Formulation, Classification of Placement Algorithms, Simulation Based Placement Algorithms, Partitioning Based Placement Algorithms, Performance Driven Placement. **Routing** -Global Routing, Problem Formulation, Classification of Global Routing Algorithms, Maze Routing Algorithms, Line-Probe Algorithms, Shortest Path Based Algorithms. Steiner Tree based Algorithms Integer Programming Based Approach, Performance Driven Routing.

UNIT – 4 Simulation, Logic Synthesis and Verification

Simulation- Gate-level Modeling and Simulation, Switch-level Modeling and Simulation. **Logic Synthesis and Verification** - Introduction to Combinational Logic Synthesis, Binary-decision Diagrams, Two-level Logic Synthesis. **High-level Synthesis-** Hardware Models for High level Synthesis, Internal Representation of the Input Algorithm, Allocation, Assignment and Scheduling

UNIT – 5

MCMs-VHDL-Verilog-implementation of simple circuits using VHDL

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Text Books:

1. N.A. Sherwani, “Algorithms for VLSI Physical Design Automation”.
2. S.H. Gerez, “Algorithms for VLSI Design Automation”, Wiley, (1999).

Reference Books:

1. Devadas, S. A., Abhijith Ghosh, A., and Keutzer, K., Logic Synthesis, Kluwer Academic, (1998).
2. Pan, D.Z., VLSI Physical Design Automation, The University of Texas at Austin, (2015).
3. Nowick, S. M., Bhardwaj, K. Computer-Aided Design of Digital Systems, Columbia University, (2016).

CO-PO Mapping:

1: Slight (Low) 2: Moderate (Medium) 3: Substantial (High) '-': No Correlation

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	2	1	3							1		
CO2	2	2	-							3		
CO3	2	-	3							1		
CO4	2	2	-							1		
CO5	3	-	-							2		

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Regulation GRMT-20	Godavari Institute of Engineering & Technology (Autonomous)	I M.Tech. I Sem (1 st Semester)			
Course Code	PROGRAMMING LANGUAGES FOR EMBEDDED SYSTEMS (Professional Elective – II)				
Teaching	Total Contact Hours-45	L	T	P	C
Prerequisites: Strong basis of digital electronics, basic computer engineering, strong computer architecture, communication systems, assembler language, C language.		3	-	-	3

Course Objectives:

1. To have knowledge about the basic working of a microcontroller system and its programming in assembly language.
2. To provide experience to integrate hardware and software for microcontroller applications systems.
3. To perform effectively as entry level Embedded Systems professionals.
4. To develop and maintain applications written using Embedded C.
5. To independently design and develop a hardware platform encompassing a microcontroller and peripherals.

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CO1:	Develop experience in assembler and C programming languages
CO2:	Write an embedded C application of moderate complexity
CO3:	Develop and analyze algorithms in C++
CO4:	Differentiate interpreted languages from compiled languages
CO5:	Build embedded system solutions with the help of common hardware interface units

UNIT-1 Embedded 'C' Programming

Bitwise operations, Dynamic memory allocation, OS services. Linked stack and queue, Sparse matrices, Binary tree. Interrupt handling in C, Code optimization issues. Embedded Software Development Cycle and Methods (Waterfall, Agile).

UNIT – 2 Object Oriented Programming

Introduction to procedural, modular, object-oriented and generic programming techniques, Limitations of procedural programming, objects, classes, data members, methods, data encapsulation, data abstraction and information hiding, inheritance, polymorphism.

UNIT – 3 CPP Programming

'cin', 'cout', formatting and I/O manipulators, new and delete operators, Defining a class, data members and methods, 'this' pointer, constructors, destructors, friend function, dynamic memory allocation.

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING**M.Tech - VLSI & Embedded Systems Course Structure and Syllabus: (2020-21)****UNIT – 4 Overloading and Inheritance**

Need of operator overloading, overloading the assignment, Overloading using friends, type conversions, single inheritance, base and derived classes, friend Classes, types of inheritance, hybrid inheritance, multiple inheritance, virtual base class, Polymorphism, virtual functions.

UNIT – 5

Templates: Function template and class template, member function templates and template arguments. Exception Handling: syntax for exception handling code: try-catch- throw, Multiple Exceptions. Scripting Languages: Overview of Scripting Languages – PERL, CGI, VB Script, Java Script. PERL: Operators, Statements Pattern Matching etc. Data Structures, Modules, Objects, Tied Variables, Inter process Communication Threads, Compilation & Line Interfacing.

Text Books:

1. Michael J. Pont, “Embedded C”, Pearson Education, 2nd Edition, 2008.
2. Randal L. Schwartz, “Learning Perl”, O’Reilly Publications, 6th Edition 2011.

Reference Books:

1. Michael Berman, “Data structures via C++”, Oxford University Press, 2002
2. Robert Sedgewick, “Algorithms in C++”, Addison Wesley Publishing Company, 1999
3. Abraham Silberschatz, Peter B, Greg Gagne, “Operating System Concepts”, John Willey & Sons, 2005 Kaufmann.

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
M.Tech - VLSI & Embedded Systems Course Structure and Syllabus: (2020-21)
CO-PO Mapping:
1: Slight (Low) 2: Moderate (Medium) 3: Substantial (High) '-': No Correlation

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	2	1	3							1		
CO2	2	2	-							3		
CO3	2	-	3							1		
CO4	2	2	-							1		
CO5	3	-	-							2		

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
M.Tech - VLSI & Embedded Systems Course Structure and Syllabus: (2020-21)

Regulation GRMT-20	Godavari Institute of Engineering & Technology (Autonomous)	I M.Tech. I Sem (1 st Semester)			
Course Code	ADVANCED COMPUTER ARCHITECTURE (Professional Elective – II)				
Teaching	Total contact hours- 45	L	T	P	C
Prerequisites: Knowledge of Logic Gates, Relays, Registers, Counter, Sensors Interfacing, Computer Architecture and Organization.		3	-	-	3

Course Objectives:

1. To understand the basic concepts of parallel execution.
2. To develop understanding with pipelining based parallelism and its hazards.
3. To develop understanding with hardware & software based ILP exploitation.
4. To develop expertise with multi-processor and multi-threading-based parallelism.
5. To understand various interconnects techniques used in multi-processor parallelism.

Course Outcomes:

On Completion of the course, the students will be able to	
CO1:	Understand the need of parallel execution and its challenges.
CO2:	Learn pipelining-based parallelization techniques.
CO3:	Apply hardware and software based ILP techniques while programming.
CO4:	Analyze multi-processor and multi-threading techniques for speedup.
CO5:	Learn the importance of interconnection techniques in multi-processor system.

UNIT – 1 Fundamentals of Computer Design

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Fundamentals of Computer design, Changing faces of computing and task of computer designer, Technology trends, Cost price and their trends, measuring and reporting performance, Quantitative principles of computer design, Amdahl's law. Instruction set principles and examples- Introduction, Classifying instruction set, Memory addressing, Type and size of operands, Operations in the instruction set.

UNIT – 2 Pipelines

Introduction, Basic RISC instruction set, Simple implementation of RISC instruction set, Classic five stage pipelined RISC processor, Basic performance issues in pipelining, Pipeline hazards, Reducing pipeline branch penalties. Memory Hierarchy Design: Introduction, Review of ABC of cache, Cache performance, Reducing cache miss penalty, Virtual memory.

UNIT – 3 Instruction Level Parallelism (ILP)-Hardware Approach

Instruction Level parallelism, Dynamic scheduling, Dynamic scheduling using Tomasulo's approach, Branch prediction, High performance instruction delivery- Hardware based speculation.

ILP Software Approach: Basic compiler level techniques, Static branch prediction, VLIW approach, Exploiting ILP, Parallelism at compile time, Cross cutting issues - Hardware verses Software.

UNIT – 4 Multi Processors and Thread Level Parallelism

Multi Processors and Thread level Parallelism- Introduction, Characteristics of application domain, Systematic shared memory architecture, Distributed shared memory architecture, Synchronization.

UNIT – 5 Inter Connection and Networks

Introduction, Interconnection network media, Practical issues in interconnecting networks, Examples of inter connection, Cluster, Designing of clusters. Intel Architecture: Intel IA-64 ILP in embedded and mobile markets Fallacies and pit falls.

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Text Books:

1. Computer Architecture: A Quantitative Approach, John L. Hennessy, David A. Patterson –3rdEdition, an Imprint of Elsevier.

Reference Books:

1. Modern Processor Design: Fundamentals of Super Scalar Processors, John P. Shen and Miikko H. Lipasti.
2. Computer Architecture and Parallel Processing - Kai Hwang, Faye A.Brigs., MC Graw Hill.
3. Advanced Computer Architecture - A Design Space Approach, DezsoSima, Terence Fountain, PeterKacsuk, Pearson Ed.

Web Links:

1. <https://nptel.ac.in/courses/106/103/106103206/>
2. https://swayam.gov.in/nd1_noc19_cs62/preview
3. <http://course.ece.cmu.edu/~ece447/s13/lib/exe/fetch.php?media=onur-447-spring13-lecture33-heterogeneousmulticore-afterlecture.pdf>
4. <https://www.ee.iitb.ac.in/~viren/Courses/2015/CS683.htm>

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M.Tech - VLSI & Embedded Systems Course Structure and Syllabus: (2020-21)
CO-PO Mapping:
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	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	2	1	3	-	1	1	1	-	-	-	1	3
CO2	2	1	1	-	-	-	1	2	-	2	-	-
CO3	2	-	3	2	1	2	2	-	3	-	2	-
CO4	1	2	-	-	-	2	3	3	2	1	-	3
CO5	3	-	-	2	-	1	-	2	-	2	-	-

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
M.Tech - VLSI & Embedded Systems Course Structure and Syllabus: (2020-21)

Regulation GRMT-20	Godavari Institute of Engineering & Technology (Autonomous)	I M.Tech. I Sem (1 st Semester)			
Course Code	EMBEDDED SYSTEM DESIGN (Professional Elective – II)				
Teaching	Total contact hours- 45	L	T	P	C
Prerequisites: Knowledge of memory devices, Software tools, Embedded processors		3	-	-	3

Course Objectives:

The main objectives of this course are given below:

1. To Define an Embedded System and understand the Embedded system design flow.
2. To understand Embedded Hardware building blocks and various Embedded Processor architecture models
3. To understand the device driver concepts and able to design various device drivers.
4. To know the importance of testing an embedded system.
5. To understand the use of various ECAD tools in the design of the embedded systems

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING**M.Tech - VLSI & Embedded Systems Course Structure and Syllabus: (2020-21)****Course Outcomes:**

On Completion of the course, the students will be able to	
CO1:	Apply processor based embedded system design concepts to develop an embedded system.
CO2:	Analyse and understand the hardware requirement of an embedded system
CO3:	Implement a device driver
CO4:	Design and Test an embedded system using appropriate software tools and hardware
CO5:	Design a processor core based embedded system

UNIT-I: Introduction

An Embedded System-Definition, Examples, Current Technologies, Integration in system Design, Embedded system design flow, hardware design concepts, software development, processor in an embedded system and other hardware units, introduction to processor based embedded system design concepts.

UNIT-II: Embedded Hardware

Embedded hardware building blocks, Embedded Processors – ISA architecture models, Internal processor design, processor performance, Board Memory – ROM, RAM, Auxiliary Memory, Memory Management of External Memory, Board Memory and performance. Embedded board Input / output – Serial versus Parallel I/O, interfacing the I/O components, I/O components and performance, Board buses – Bus arbitration and timing, Integrating the Bus with other board components, Bus performance.

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UNIT-III: Embedded Software

Device drivers, Device Drivers for interrupt-Handling, Memory device drivers, On-board bus device drivers, Board I/O drivers, Explanation about above drivers with suitable examples. Embedded operating systems – Multitasking and process Management, Memory Management, I/O and file system management, OS standards example – POSIX, OS performance guidelines, Board support packages, Middleware and Application Software – Middle ware, Middleware examples, Application layer software examples.

UNIT-IV: Embedded System Design, Development, Implementation and Testing

Embedded system design and development lifecycle model, creating an embedded system architecture, introduction to embedded software development process and tools- Host and Target machines, linking and locating software, Getting embedded software into the target system, issues in Hardware-Software design and co-design. Implementing the design-The main software utility tool, CAD and the hardware, Translation tools, Debugging tools, testing on host machine, simulators, Laboratory tools, System Boot-Up.

UNIT-V: Embedded System Design-Case Studies

Case studies- Processor design approach of an embedded system –Power PC Processor based and Micro Blaze Processor based Embedded system design on Xilinx platform-NiosII Processor based Embedded system design on Altera platform-Respective Processor architectures should be taken into consideration while designing an Embedded System.

Text Books:

1. Tammy Noergaard “Embedded Systems Architecture: A Comprehensive Guide for Engineers and Programmers”, Elsevier(Singapore) Pvt. Ltd. Publications, 2005.
2. Frank Vahid, Tony D. Givargis, “Embedded system Design: A Unified Hardware/Software Introduction”, John Wily & Sons Inc.2002.

Reference Books:

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
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1. Peter Marwedel, "Embedded System Design", Science Publishers, 2007.
2. Arnold S Burger, "Embedded System Design", CMP.
3. Rajkamal, "Embedded Systems: Architecture, Programming and Design", TMH Publications, Second Edition, 2008.

CO-PO Mapping:
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	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	2	1	3	-	1	1	1	-	-	-	1	3
CO2	2	1	1	-	-	-	1	2	-	2	-	-
CO3	2	-	3	2	1	2	2	-	3	-	2	-
CO4	1	2	-	-	-	2	3	3	2	1	-	3
CO5	3	-	-	2	-	1	-	2	-	2	-	-

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M.Tech - VLSI & Embedded Systems Course Structure and Syllabus: (2020-21)

Regulation GRMT-20	Godavari Institute of Engineering & Technology (Autonomous)	I M.Tech. I Sem (1 st Semester)			
Course Code	RESEARCH METHODOLOGY				
Teaching	Total Contact Hours-30	L	T	P	C
Pre requisites: None		2	-	-	2

Course Objectives:

1. To give an overview of the research methodology and explain the technique of defining a research problem
2. To explain the functions of the literature review in research.
3. To explain carrying out a literature search, its review, developing theoretical and conceptual frameworks and writing a review.
4. To explain various research designs and their characteristics.
5. To explain various forms of the intellectual property, its relevance and business impact in the changing global business environment

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING**M.Tech - VLSI & Embedded Systems Course Structure and Syllabus: (2020-21)****Course Outcomes:**

On Completion of the course, the students will be able to	
CO1:	Understand research problem formulation
CO2:	Analyze research related information
CO3:	Follow research ethics
CO4:	Understand that today's world is controlled by Computer, Information Technology, but tomorrow world will be ruled by ideas, concept, and creativity
CO5:	Understand that IPR protection provides an incentive to inventors for further research work and investment in R & D

UNIT-1

Meaning of research problem, Sources of research problem, Criteria Characteristics of a good research problem, Errors in selecting a research problem, Scope and objectives of research problem. Approaches of investigation of solutions for research problem, data collection, analysis, interpretation, Necessary instrumentations.

UNIT - 2

Effective literature studies approaches, analysis Plagiarism, Research ethics. Effective technical writing, how to write report, Paper Developing a Research Proposal, Format of research proposal, presentation and assessment by a review committee.

UNIT - 3

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING**M.Tech - VLSI & Embedded Systems Course Structure and Syllabus: (2020-21)**

Nature of Intellectual Property: Patents, Designs, Trade and Copyright. Process of Patenting and Development: technological research, innovation, patenting, development.

International Scenario: International cooperation on Intellectual Property. Procedure for grants of patents, Patenting under PCT.

UNIT – 4

Patent Rights: Scope of Patent Rights. Licensing and transfer of technology. Patent information and databases. Geographical Indications.

UNIT – 5

New Developments in IPR: Administration of Patent System. New developments in IPR; IPR of Biological Systems, Computer Software etc. Traditional knowledge Case Studies, IPR and IITs.

Text Books:

1. Stuart Melville and Wayne Goddard, "Research methodology: an introduction for science & engineering students".
2. Wayne Goddard and Stuart Melville, "Research Methodology: An Introduction".
3. Ranjit Kumar, 2nd Edition, "Research Methodology: A Step by Step Guide for beginners".
4. Halbert, "Resisting Intellectual Property", Taylor & Francis Ltd ,2007.

Reference Books:

1. Mayall, "Industrial Design", McGraw Hill, 1992.
2. Niebel, "Product Design", McGraw Hill, 1974.
3. Asimov, "Introduction to Design", Prentice Hall, 1962.
4. Robert P. Merges, Peter S. Menell, Mark A. Lemley, "Intellectual Property in New Technological Age", 2016.
5. T. Ramappa, "Intellectual Property Rights Under WTO", S. Chand, 2008

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CO-PO Mapping:
1: Slight (Low) 2: Moderate (Medium) 3: Substantial (High) '-': No Correlation

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	2	1	3	-	-	-	-	-	-	1	-	-
CO2	2	2	-	-	-	-	-	-	-	3	-	-
CO3	2	-	3	-	-	-	-	-	-	1	-	-
CO4	2	2	-	-	-	-	-	-	-	1	-	-
CO5	3	-	-	-	-	-	-	-	-	2	-	-

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M.Tech - VLSI & Embedded Systems Course Structure and Syllabus: (2020-21)

Regulation GRBT-20	Godavari Institute of Engineering & Technology (Autonomous)	I M.Tech. I Sem (1 st Semester)			
Course Code	RTL SIMULATION AND SYNTHESIS WITH PLDs Lab				
Teaching	Total Contact Hours – 30	L	T	P	C
Prerequisites: Knowledge of Digital Circuit Design and VHDL/Verilog Programming.		0	0	4	2

Course Objectives:

1. To introduce Verilog HDL for the design and functionality verification of a digital circuit.
2. To understand the design of data path and control circuits for sequential machines.
3. To introduce the concept of realizing a digital circuit using PLDs.

Course Outcomes:

On Completion of the course, students will be able to	
CO1:	Develop the Verilog HDL to design a digital circuit.
CO2:	Identify, formulate, solve and implement problems in signal processing, communication Systems etc using RTL design tools.
CO3:	Use EDA tools like Cadence, Mentor Graphics and Xilinx.
CO4:	Verify the functionality of the digital designs using PLDs.

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List of Experiments:

- 1) Verilog implementation of
 - a. 8:1 Mux/ Demux
 - b. Full Adder, 8-bit Magnitude comparator
 - c. 3-bit Synchronous Counters
 - d. Parity generator
- 2) Sequence generator/detectors, Synchronous FSM – Mealy and Moore machines.
- 3) Vending machines - Traffic Light controller, ATM, elevator control.
- 4) PCI Bus & arbiter and downloading on FPGA.
- 5) UART/ USART implementation in Verilog
- 6) Realization of single port SRAM in Verilog
- 7) Verilog implementation of Arithmetic circuits like serial adder/ subtractor, parallel adder/subtractor, serial/parallel multiplier.
- 8) Discrete Fourier transform/Fast Fourier Transform algorithm in Verilog.

Text Books:

4. Verilog HDL-A Guide to Digital Design and Synthesis, Samir Palnitkar, 2ndEdition, 2003.
5. Fundamentals of Logic Design, Charles H. Roth, 5thEdition, Cengage Learning, 2010.
6. Verilog HDL Synthesis - A Practical Primer, Bhasker J, 1stedition, 1998.

Reference Books:

4. Digital principles and Design, Donald D Givone, TMH, 2016.
5. Designing with FPGAs & CPLDs, Bob Zeidman, CMP Books, 2002.
6. Modern Digital Design, Richard S. Sandige, MGH, International Editions, 1990.

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CO-PO Mapping

1: Slight (Low) 2: Moderate (Medium) 3: Substantial (High) '-' : No Correlation

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	2	2	2		2					2		2
CO2	2	-	-		2					2		2
CO3	2	2	2		2					2		2
CO4	3	-	2		2					2		2

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M.Tech - VLSI & Embedded Systems Course Structure and Syllabus: (2020-21)

Regulation GRBT-20	Godavari Institute of Engineering & Technology (Autonomous)	I M.Tech. I Sem (1 st Semester)			
Course Code	MICROCONTROLLERS AND PROGRAMMABLE DIGITAL SIGNAL PROCESSORS LAB				
Teaching	Total Contact Hours – 30	L	T	P	C
Prerequisites: Knowledge of ARM microcontrollers and TMS320C6713 DSP processors.		0	0	4	2

Course Objectives:

1. To perform interfacing of various devices with ARM using Embedded C.
2. To develop program for implementation of interrupts and serial communications.
3. To implement digital signal processing algorithms in MATLAB and C.
4. To understand the real-time operation of digital filters.

Course Outcomes:

On Completion of the course, students will be able to	
CO1:	Install, configure and utilize tool sets for developing applications based on ARM processor Core SoC and DSP processor.
CO2:	Develop prototype codes using commonly available on and off chip peripherals on the Cortex M3 and DSP development boards.
CO3:	Develop several interfacing methods to control the peripherals.
CO4:	Develop C code for filtering applications.

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING**M.Tech - VLSI & Embedded Systems Course Structure and Syllabus: (2020-21)****List of Experiments:**

Part A) Experiments to be carried out on Cortex-M3 development boards and using GNU Tool chain

1. Blink an LED with software delay, delay generated using the Sys Tick timer.
2. System clock real time alteration using the PLL modules.
3. Control intensity of an LED using PWM implemented in software and hardware.
4. Control an LED using switch by polling method, by interrupt method and flash the LED once every five switch presses.
5. Take analog readings on rotation of rotary potentiometer connected to an ADC channel.
6. Temperature indication on an RGB LED.
7. Mimic light intensity sensed by the light sensor by varying the blinking rate of an LED.
8. Evaluate the various sleep modes by putting core in sleep and deep sleep modes.
9. System reset using watchdog timer in case something goes wrong.
10. Sample sound using a microphone and display sound levels on LEDs.

Part B) Experiments to be carried out on DSP C6713 evaluation kits and using Code Composer Studio (CCS)

1. To develop an assembly code and C code to compute Euclidian distance between any two points
2. To develop assembly code and study the impact of parallel, serial and mixed execution
3. To develop assembly and C code for implementation of convolution operation
4. To design and implement filters in C to enhance the features of given input sequence/signal

Text Books:

1. The definitive guide to ARM Cortex-M3, Joseph Yiu, Elsevier, 2nd Edition.
2. Digital Signal Processors: Architecture, Programming and Applications, Venkatramani B. and Bhaskar M., TMH, 2nd Edition.
3. ARM System Developer's Guide: Designing and Optimizing, Sloss Andrew N, Symes Dominic, Wright Chris, Morgan Kaufman Publication.

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
M.Tech - VLSI & Embedded Systems Course Structure and Syllabus: (2020-21)
Reference Books:

1. ARM System-on-Chip Architecture, Steve Furber, Pearson Education.
2. Embedded System Design, Frank Vahid and Tony Givargis, Wiley.
3. Technical references and user manuals on www.arm.com.

CO-PO Mapping:
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	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	2	2	2	-	2	-	-	-	-	2	-	2
CO2	2	-	-	-	2	-	-	-	-	2	-	2
CO3	2	2	2	-	2	-	-	-	-	2	-	2
CO4	3	-	2	-	2	-	-	-	-	2	-	2

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
M.Tech - VLSI & Embedded Systems Course Structure and Syllabus: (2020-21)
I YEAR II SEMESTER

Regulation GRMT-20	Godavari Institute of Engineering & Technology (Autonomous)	I MTech. II Sem (2 nd Semester)			
Course Code	Analog and Digital CMOS VLSI Design				
Teaching	Totalcontacthours-45	L	T	P	C
Prerequisites: Knowledge of CMOS Digital integrated circuit, Basic semiconductor memories, Analog IC design, Op Amps.		3	-	-	3

Course Objectives:

1. To teach fundamentals of CMOS Digital integrated circuit design.
2. To teach the fundamentals of Dynamic logic circuits and basic semiconductor memories.
3. To understand design concepts, issues and trade off involved in analog IC design.
4. To learn about design of CMOS Op Amps and measurement techniques of OP Amp.

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Course Outcomes:

On Completion of the course, the students will be able to	
CO1:	Identify the trade-offs involved in analog integrated circuit design.
CO2:	Analyse complex engineering problems critically in the domain of analog IC design for conducting research.
CO3:	Demonstrate advanced knowledge in Static and dynamic characteristics of CMOS, Alternative CMOS Logics, Estimation of Delay and Power, Adders Design.
CO4:	Solve engineering problems for feasible and optimal solutions in the core area of digital ICs.
CO5:	Understand and appreciate the importance of noise and distortion in analog circuits.

Unit – 1 Digital CMOS Design

Basic MOS structure and its static behaviour, Quality metrics of a digital design: Cost, Functionality, Robustness, Power, and Delay, Stick diagram and Layout, Wire delay model. Inverter: Static CMOS inverter, Switching threshold and noise margin concepts and their Evaluation, Dynamic behaviour, Power consumption.

Unit – 2 Physical Design Flow

Floor planning, Placement, Routing, CTS, Power analysis and IR drop estimation- Static and Dynamic, ESD protection-human body model, Machine model. Combinational logic: Static CMOS design, Logic effort, Rationed logic, Pass transistor logic, Dynamic logic, Speed and power dissipation in dynamic logic, Cascading dynamic gates, CMOS transmission gate logic.

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING**M.Tech - VLSI & Embedded Systems Course Structure and Syllabus: (2020-21)****Unit – 3 Sequential Logic**

Static latches and registers, Bi-stability principle, MUX based latches, Static SR flip-flops, Master-slave edge-triggered register, Dynamic latches and registers, Concept of pipelining, Pulse registers, Non-bistable sequential circuit. Advanced technologies: Giga-scale dilemma, Short channel effects, High-k, Metal Gate Technology, FinFET, TFET etc.

Unit – 4 Single Stage Amplifier

CS stage with resistance load, Divide connected load, Current source load, Triode load, CS stage with source degeneration, Source follower, Common gate stage, Cascade stage, Choice of device models. Differential Amplifiers: Basic difference pair, Common mode response, Differential pair with MOS loads, Gilbert cell.

Unit – 5 Passive and Active Current Mirrors

Basic current mirrors, Cascade mirrors, Active current mirrors. Frequency response of CS stage: Source follower, Common gate stage, Cascade stage and Difference pair, Noise. Operational amplifiers: One stage OPAMP, Two stage OPAMP, Gain boosting, Common mode feedback, Slew rate, PSRR, Compensation of 2 stage OPAMP.

Text Books:

1. Digital Integrated circuits: A design perspective, J P Rabaey, A P Chandrakasan, B Nikolic, Prentice Hall electronics and VLSI series, 2nd Edition.
2. CMOS Circuit Design, Layout, and Simulation, Baker, Li, Boyce, Wiley, 2nd Edition.
3. Design of Analog CMOS Integrated Circuits, Behzad Razavi, TMH, 2007.

Reference Books:

1. CMOS Analog Circuit Design - Phillip E. Allen and Douglas R. Holberg, Oxford, 3rd Edition.
2. CMOS circuit Design, Layout and Simulation, R J Baker, IEEE Inc., 2008.
3. CMOS Digital Integrated Circuits, Analysis and Design - Kang, S. and Leblebici, Y., TMH, 3rd Edition.

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
M.Tech - VLSI & Embedded Systems Course Structure and Syllabus: (2020-21)
CO-PO Mapping:
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CO1	2	1	3	-	1	1	1	-	-	-	1	-
CO2	2	1	1	-	-	-	1	2	-	2	-	-
CO3	-	-	3	2	1	-	2	-	-	-	2	-
CO4	1	2	-	-	-	-	3	-	2	1	-	-
CO5	3	-	-	2	-	1	-	2	-	2	-	-

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
M.Tech - VLSI & Embedded Systems Course Structure and Syllabus: (2020-21)

Regulation GRMT-20	Godavari Institute of Engineering & Technology (Autonomous)	I M.Tech. II Sem (2 nd Semester)			
Course Code	REAL TIME OPERATING SYSTEMS				
Teaching	Totalcontacthours-45	L	T	P	C
Prerequisites: Knowledge of Computer Architecture and Organization and Logic Design.		3	-	-	3

Course Objectives:

1. To learn the basic designs using an RTOS.
2. To know the functions and types of RTOS for embedded systems.
3. To analyze the issues in real time operating systems.
4. To understand the programming concepts of RTOS.
5. To analyze the operating system software.

Course Outcomes:
On Completion of the course, the students will be able to

CO1:	Illustrate real time programming concepts.
CO2:	Apply RTOS functions to implement embedded applications.
CO3:	Understand Interrupt service mechanism and I/O subsystem design.
CO4:	Describe various types of Memory Management of RTOS.
CO5:	Understand fundamentals of design consideration for embedded applications.

UNIT – 1 Introduction to Real-Time Operating Systems

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Defining an RTOS, The scheduler, Kernel Objects and services, Key characteristics of an RTOS. Task- Defining a Task, Task States and Scheduling, Typical Task Operations, Typical Task Structure, Synchronization, Communication and Concurrency.

UNIT – 2 Semaphores & Message Queues

Semaphores - Defining Semaphores, Typical Semaphore Operations, Typical Semaphore Use. Message Queues - Defining Message Queues, Message Queue States, Message Queue Content, Message Queue Storage, Typical Message Queue Operations, Typical Message Queue Use, Pipes, Event Registers, Signals and condition Variables.

UNIT – 3 Interrupts & Sub systems

Exceptions and Interrupts - Exceptions and Interrupts, Applications of exceptions and interrupts, Closer look at exceptions and interrupts, Processing general exceptions, Nature of spurious Interrupts. Timer and Timer Services – Real time clocks and System clocks, Programmable Interval Timers, Timer Interrupt Service Routines. I/O Subsystems - I/O concepts, I/O subsystems.

UNIT –4 Memory management of RTOS

Memory Management -Dynamic Memory Allocation in Embedded Systems, Fixed-Size Memory management in Embedded Systems, Blocking Vs Non-Blocking Memory Functions, Hardware Memory Management Units. Modularizing an application for concurrency-An outside-in approach to decompose the Applications, Guidelines and Recommendations for identifying Concurrency, Schedulability Analysis.

UNIT – 5 Synchronization and Communication

Synchronization and Communication - Synchronization, Communication, Resource synchronization methods, Critical section, Common practical design patterns, Specific solution Design patterns. Common Design Problems - Resource classification, Deadlocks, Priority inversion.

Text Books:

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

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1. Real-Time Concepts for Embedded Systems, Qing Li, Caroline Yao (2003), CMP Books.

Reference Books:

1. Real-Time Systems: Scheduling, Analysis and Verification, AlbertCheng, Wiley Interscience (2002).
2. Real-Time Systems: Design Principles for Distributed Embedded Applications, Hermann Kopetz, Kluwer (1997).
3. Handbook of Real-Time Systems, InsupLee, JosephLeung, and SangSon,(2008).
4. Real-Time Systems, Chapman and Hall. Krishna and Kang G Shin, McGraw Hill(2001).

Web Links:

1. <https://realtimelogic.com>.
2. <https://www.freertos.org>
3. RTOS for ARM-LINKS.
4. RTOS and embedded Linux OS from LYNEX works.
5. RTOS embedded system glossary.

CO-PO Mapping:

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1: Slight (Low) 2: Moderate (Medium) 3: Substantial (High) '-' : No Correlation

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	2	1	3	-	1	1	1	-	-	-	1	3
CO2	2	1	1	-	-	-	1	2	-	2	-	-
CO3	2	-	3	2	1	2	2	-	3	-	2	-
CO4	1	2	-	-	-	2	3	3	2	1	-	3
CO5	3	-	-	2	-	1	-	2	-	2	-	-

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Regulation GRMT-20	Godavari Institute of Engineering & Technology (Autonomous)	I M.Tech. II Sem (2 nd Semester)			
Course Code	SYSTEM DESIGN WITH EMBEDDED LINUX (Professional Elective – III)				
Teaching	Total contact hours - 45	L	T	P	C
Prerequisites: Knowledge of Embedded systems, Operating systems, C and C++ language.		3	-	-	3

Course Objectives:

1. To understand the embedded Linux development model.
2. To be able to write and debug applications in embedded Linux.
3. To be able to write and debug drivers in embedded Linux.
4. To be able to understand Linux BSP for a hardware platform.
5. To be able to create Linux BSP for a hardware platform.

Course Outcomes:

On Completion of the course, the students will be able to	
CO1:	Understand embedded Linux development model.
CO2:	Write and debug applications and drivers in embedded Linux.
CO3:	Discuss embedded storage and drivers for real time applications.
CO4:	Learn real-time Linux and programming.
CO5:	Understand and create Linux BSP for a hardware platform.

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UNIT – 1 Embedded Linux

Embedded Linux, Vendor Independence, Time to Market, Varied Hardware Support, Open Source, Standards (POSIX®) Compliance, Embedded Linux Versus Desktop Linux, Embedded Linux Distributions, Blue Cat Linux, Cadenux , Denx, Embedded Debian (Emdebian), ELinOS (SYSGO), Metrowerks, Monta Vista Linux, RT Linux Pro, Time Sys Linux.

UNIT – 2 Embedded Linux Architecture

Embedded Linux Architecture, Real-Time Executive, Monolithic Kernels, Micro kernel. Kernel Architecture – HAL, Memory manager, Scheduler, File System, I/O and Networking subsystem, IPC, User space, Start-up sequence, Boot Loader Phase, Kernel Start-Up, User Space Initialization.

UNIT – 3 Board Support Package Embedded Storage

MTD, Architecture, Drivers, Embedded File System. Embedded Drivers: Serial, Ethernet, I2C, USB, Timer, Kernel Modules.

UNIT – 4 Real Time Linux

Porting Applications, Architectural Comparison, Application Porting Roadmap, Programming with Pthreads, Operating System Porting Layer (OSPL), Kernel API Driver, Real-Time Linux: Linux and Real time, Programming, Hard Real-time Linux.

UNIT – 5 Building and Debugging

Kernel, Building the Kernel, Building Applications, Building the Root File System, Integrated Development Environment, Debugging Virtual Memory Problems, Kernel Debuggers, Root file system. Embedded Graphics - Graphics System, Linux Desktop Graphics, Embedded Linux Graphics, Embedded Linux Graphics Driver, Windowing Environments, Toolkits, and Applications, Case study of uClinux.



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Text Books:

1. Building Embedded Linux Systems – Karim Yaghmour, O'Reilly & Associates.
2. Embedded Linux System Design and Development - P. Raghvan, Amol Lad, Sriram Neelakandan, Auerbach Publications.

Reference Books:

1. Embedded Linux Primer: A Practical Real-World Approach - Christopher Hallinan, Prentice Hall, 2nd Edition, 2010.
2. Exploring Beagle Bone: Tools and Techniques for Building with Embedded Linux - Derek Molloy, Wiley, 1st Edition, 2014.

Web Links:

1. <https://nptel.ac.in/courses/106105159/>
2. <https://nptel.ac.in/courses/106/105/106105193/>
3. <https://freevideolectures.com/course/2341/embedded-systems>
4. <https://nptel.ac.in/courses/117106113/>
5. <https://nptel.ac.in/courses/108102045/>

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CO-PO Mapping:
1: Slight (Low) 2: Moderate (Medium) 3: Substantial (High) '-' : No Correlation

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	2	1	3	-	1	1	1	-	-	-	1	3
CO2	2	1	1	-	-	-	1	2	-	2	-	-
CO3	2	-	3	2	1	2	2	-	3	-	2	-
CO4	1	2	-	-	-	2	3	3	2	1	-	3
CO5	3	-	-	2	-	1	-	2	-	2	-	-

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M.Tech - VLSI & Embedded Systems Course Structure and Syllabus: (2020-21)

Regulation GRMT-20	Godavari Institute of Engineering & Technology (Autonomous)	I M.Tech. II Sem (2 nd Semester)			
CourseCode	COMMUNICATION BUSES & INTERFACES (Professional Elective – III)				
Teaching	Total contact hours-45	L	T	P	C
Prerequisites: Knowledge of Computer Networks and Communication protocols.		3	-	-	3

Course Objectives:????

Course Outcomes:

On completion of the course, the students will be able to	
CO1:	Select a particular serial bus suitable for a particular application.
CO2:	Develop APIs for configuration, reading and writing data onto serial bus.
CO3:	Design and develop peripherals that can be interfaced to desired serial bus.

UNIT – 1 Serial Buses

Cables, Serial buses, serial versus parallel, Data and Control Signal- data frame, data rate, features Limitations and applications of RS232, RS485, I2C, SPI.

UNIT – 2 CAN

ARCHITECTURE- ISO 11898-2, ISO 11898-3, Data Transmission- ID allocation, Bit timing, Layers-Application layers, Object layer, Transfer layer, Physical layer, Frame formats- Data frame, Remote frame, Error frame, Over load frame, Ack slot, Inter frame spacing, Bit spacing, Applications.

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UNIT – 3 PCIe

Revision, Configuration space- configuration mechanism, Standardized registers, Bus enumeration, Hardware and Software implementation, Hardware protocols, Applications.

UNIT – 4 USB

Transfer Types- Control transfers, Bulk transfer, Interrupt transfer, Isochronous transfer. Enumeration-Device detection, Default state, Addressed state, Configured state, enumeration sequencing. Descriptor types and contents- Device descriptor, configuration descriptor, Interface descriptor, Endpoint descriptor, String descriptor. Device driver.

UNIT – 5 Data Streaming

Serial Communication Protocol - Serial Front Panel Data Port(SFPDP) configurations, Flow control, serial FPDP transmission frames, fiber frames and copper cable.

Text Books:

1. A Comprehensive Guide to controller Area Network – Wilfried Voss, Copperhill Media Corporation, 2nd edition, 2005.
2. Serial Port Complete-COM Ports, USB Virtual Com Ports and Ports for Embedded Systems- Jan Axelson, Lakeview Research, 2nd Edition.

Reference Books:

1. USB Complete – Jan Axelson, Penram Publications.
2. PCI Express Technology – Mike Jackson, Ravi Budruk, Mindshare Press.

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	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	2	2	-	-	-	-	-	-	-	2	-	-
CO2	2	2	-	-	-	-	-	-	-	2	-	-
CO3	2	2	-	-	-	-	-	-	-	2	-	-

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Regulation GRMT-20	Godavari Institute of Engineering & Technology (Autonomous)	I M.Tech. II Sem (2 nd Semester)			
CourseCode	HARDWARE SOFTWARE CO-DESIGN (Professional Elective – III)				
Teaching	Totalcontacthours-45	L	T	P	C
Prerequisites: Knowledge of Computer Architecture & Organization, Embedded System Design and Microprocessors/Controllers.		3	-	-	3

Course Objectives:

1. To introduce co-design methodology and hardware-software synthesis algorithms.
2. To understand prototyping and emulation techniques for target architecture.
3. To introduce compilation techniques and tools for embedded processor architectures.
4. To learn the issues involved in design specification and verification.
5. To learn system level specification languages for the design of embedded systems.

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CO1:	Understand the basics of Hardware Software Co-design
CO2:	How to select a target architecture and how a prototype is built and how emulation of a prototype is done.
CO3:	Acquire knowledge about compilation technologies and compiler development environment.
CO4:	Formulate design specifications and perform design verification.
CO5:	Understand the importance of system level specification languages and multi-language co-simulation.

UNIT – 1 Co-Design Issues

Co-Design Models, Architectures, Languages, A Generic Co-design Methodology.

Co-Synthesis Algorithms: Hardware software synthesis algorithms: hardware – software partitioning distributed system co-synthesis.

UNIT – 2 Prototyping and Emulation

Prototyping and emulation techniques, Prototyping and emulation environments, Future developments in emulation and prototyping architecture specialization techniques, System communication infrastructure. Target Architectures - Architecture specialization techniques, System communication infrastructure, Target architecture and application system classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.



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UNIT – 3 Compilation Techniques and Tools for Embedded Processor Architectures

Modern embedded architectures, Embedded software development needs, Compilation technologies, Practical consideration in a compiler development environment.

UNIT – 4 Design Specification and Verification

Design, Co-design, The co-design computational model, Concurrency coordinating concurrent computations, Interfacing components, Design verification, Implementation verification, Verification tools, Interface verification.

UNIT – 5 Languages for System Level Specification and Design

Languages for System Level Specification and Design-I: System level specification, design representation for system level synthesis, system level specification languages. Languages for System Level Specification and Design-II: Heterogeneous specifications and multi-language co-simulation, The cosyma system and lycos system.

Text Books:

1. Hardware / Software Co- Design Principles and Practice, Jorgen Staunstrup, Wayne Wolf – 2009, Springer.
2. Hardware / Software Co- Design, Giovanni De Micheli, Mariagiovanna Sami, 2002, Kluwer Academic Publishers.

Reference Books:

1. A Practical Introduction to Hardware/Software Co-design, Patrick R. Schaumont, 2010, Springer Publications.

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CO-PO Mapping:
1: Slight (Low) 2: Moderate (Medium) 3: Substantial (High) '-': No Correlation

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	2	1	3	-	1	1	1	-	-	-	1	3
CO2	2	1	1	-	-	-	1	2	-	2	-	-
CO3	2	-	3	2	1	2	2	-	3	-	2	-
CO4	1	2	-	-	-	2	3	3	2	1	-	3
CO5	3	-	-	2	-	1	-	2	-	2	-	-

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Regulation GRMT-20	Godavari Institute of Engineering & Technology (Autonomous)	I M.Tech. II Sem (2 nd Semester)			
CourseCode	PHYSICAL DESIGN AUTOMATION (Professional Elective – IV)				
Teaching	Totalcontacthours-45	L	T	P	C
Prerequisites: Knowledge of Integrated Circuits, digital circuit design and introduction to VLSI		3	-	-	3

Course Objectives:

1. To understand the problems arising in the physical design of VLSI circuits.
2. To develop understanding various CAD algorithms for automating the physical design process.
3. To develop understanding to modify the existing or new DSP architectures suitable for VLSI.
4. To develop understanding the concepts of folding and unfolding algorithms and applications.
5. To develop understanding low power design aspects of processors for signal processing and wireless applications.

Course Outcomes:

On Completion of the course, the students will be able to	
CO1:	Understand the relationship between design automation algorithms.
CO2:	Learn various constraints posed by VLSI fabrication and design technology.
CO3:	Adapt the design algorithms to meet the critical design parameters.
CO4:	Identify layout optimization techniques and map them to the algorithms.
CO5:	Develop proto-type EDA tool and test its efficacy.

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UNIT – 1

VLSI design Cycle, Physical Design Cycle, Design Rules, Layout of Basic Devices, and Additional Fabrication, Design styles: full custom, standard cell, gate arrays, field programmable gate arrays, sea of gates and comparison, system packaging styles, multi-chip modules. Design rules, layout of basic devices, fabrication process and its impact on physical design, interconnect delay, noise and cross talk, yield and fabrication cost.

UNIT – 2

Factors, Complexity Issues and NP-hard Problems, Basic Algorithms (Graph and Computational Geometry): graph search algorithms, spanning tree algorithms, shortest path algorithms, matching algorithms, min-cut and max-cut algorithms, Steiner tree algorithms.

UNIT – 3

Basic Data Structures, atomic operations for layout editors, linked list of blocks, bin-based methods, neighbor pointers, corner stitching, multi-layer operations.

UNIT – 4

Graph algorithms for physical design: classes of graphs, graphs related to a set of lines, graphs related to set of rectangles, graph problems in physical design, maximum clique and minimum colouring, maximum k-independent set algorithm, algorithms for circle graphs.

UNIT – 5

Partitioning algorithms: design style specific partitioning problems, group migrated algorithms, simulated annealing and evolution, and Floor planning and pin assignment, Routing and placement algorithms.

Text Books:

1. Naveed Shervani, Algorithms for VLSI Physical Design Automation, 3rd Edition, Kluwer Academic, 1999.
2. Charles J Alpert, Dinesh P Mehta, Sachin S Sapatnekar, Handbook of Algorithms for Physical Design Automation, CRC Press, 2008.

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Reference Books:

1. Sadiq M Sait, Habib Youssef, VLSI Physical Design Automation, 1999.
2. M. Sarrafzadeh and C. K. Wong, An Introduction to VLSI Physical Design, McGraw-Hill, 1996.

Web Links:

1. <https://nptel.ac.in/courses/106105161/>
2. https://swayam.gov.in/nd1_noc20_cs18/preview

CO-PO Mapping:
1: Slight (Low) 2: Moderate (Medium) 3: Substantial (High) '-': No Correlation

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	1	3	-	-	-	-	-	-	-	-	-	2
CO2	2	3	-	-	-	-	-	-	-	-	-	1
CO3	1	3	-	-	-	-	-	-	-	-	-	1
CO4	2	3	-	-	-	-	-	-	-	-	-	2
CO5	1	3	-	-	-	-	-	-	-	-	-	2

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Regulation GRMT-20	Godavari Institute of Engineering & Technology (Autonomous)	I M.Tech. II Sem (2 nd Semester)			
Course Code	SoC DESIGN (Professional Elective – IV)				
Teaching	Total contact hours - 45	L	T	P	C
Prerequisites: Knowledge of Electronics, Digital Hardware design		3	-	-	3

Course Objectives:

1. To understand how chip designers, create smart phones using SoC - System-On-Chip
2. To understand the SoC Design architecture and process
3. To understand the technologies and usage of ASICs and FPGAs
4. To understand the complete VLSI Design Flow

Course Outcomes:

On Completion of the course, the students will be able to	
CO1:	Identify and formulate a given problem in the framework of SoC based design approaches
CO2:	Design SoC based system for engineering applications
CO3:	Realize impact of SoC on electronic design philosophy and Macro-electronics thereby incline towards entrepreneurship & skill development.

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UNIT – 1 ASIC

Overview of ASIC types, design strategies, CISC, RISC and NISC approaches for SOC architectural issues and its impact on SoC design methodologies, Application Specific Instruction Processor (ASIP) concepts.

UNIT – 2 NISC

NISC Control Words methodology, NISC Applications and Advantages, Architecture Description Languages (ADL) for design and verification of Application Specific Instruction set Processors (ASIP), No-Instruction-Set-computer (NISC) - design flow, Modeling NISC architectures and systems, use of Generic Netlist Representation - A formal language for specification, compilation and synthesis of embedded processors.

UNIT – 3 Simulation

Different simulation modes, behavioral, functional, static timing, gate level, switch level, transistor/circuit simulation, design of verification vectors, Low power FPGA, Reconfigurable systems, SoC related Modeling of data path design and control logic, Minimization of interconnects impact, clock tree design issues.

UNIT – 4 Low power SoC design / Digital system

Design synergy, Low power system perspective- power gating, clock gating, adaptive voltage scaling (AVS), Static voltage scaling, Dynamic clock frequency and voltage scaling (DCFS), building block optimization, building block memory, power down techniques, power consumption verification.

UNIT – 5 Synthesis

Role and Concept of graph theory and its relevance to synthesizable constructs, Walks, trails paths, connectivity, components, mapping/visualization, nodal and admittance graph. Technology independent and technology dependent approaches for synthesis, optimization constraints, Synthesis report analysis Single core and Multi core systems, dark silicon issues, HDL coding techniques for minimization of power consumption, Fault tolerant designs.

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Text Books:

1. Hubert Kaeslin, “Digital Integrated Circuit Design: From VLSI Architectures to CMOS Fabrication”, Cambridge University Press, 2008.
2. B. Al Hashimi, “System on chip-Next generation electronics”, The IET, 2006.

Reference Books:

1. Rochit Rajsuman, “System-on- a-chip: Design and test”, Advantest America R & D Center,2000.
2. P Mishra and N Dutt, “Processor Description Languages”, Morgan Kaufmann, 2008.
3. Michael J. Flynn and Wayne Luk, “Computer System Design: System-on-Chip”, Wiley.

CO-PO Mapping:

1: Slight (Low) 2: Moderate (Medium) 3: Substantial (High) '-': No Correlation

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	2	2	-	-	-	-	-	-	-	2	-	-
CO2	2	2	-	-	-	-	-	-	-	2	-	-
CO3	2	2	-	-	-	-	-	-	-	2	-	-

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Regulation GRMT-20	Godavari Institute of Engineering & Technology (Autonomous)	I M.Tech. II Sem (2 nd Semester)			
CourseCode	LOW POWER VLSI DESIGN (Professional Elective – IV)				
Teaching	Total Contact Hours-45	L	T	P	C
Prerequisites: Knowledge of Electronics Devices and Circuits, VLSI Design, Switching Theory and Logic Design.		3	-	-	3

Course Objectives:

1. To understand the basics of low Power VLSI design.
2. To understand state-of-the art approaches to power estimation and reduction.
3. To discuss various power reduction and estimation methods.
4. To familiarize with power dissipation at all layers of design hierarchy from technology, circuit, logic, architecture and system.
5. To understand the importance of low-voltage, low-power memories and its future development.

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING**M.Tech - VLSI & Embedded Systems Course Structure and Syllabus: (2020-21)****Course Outcomes:****On Completion of the course, the students will be able to**

CO1:	Identify the sources of power dissipation in digital IC systems & understand the impact of power on system performance and reliability
CO2:	Characterize and model power consumption & understand the basic analysis methods
CO3:	Understand leakage sources and reduction techniques
CO4:	Estimate power dissipation in clock distribution and suggest methods to reduce
CO5:	Learn the design techniques low voltage and low power CMOS circuits for various applications

UNIT-1 Technology & Circuit Design Levels

Sources of power dissipation in digital ICs, degree of freedom, recurring themes in low-power, emerging low power approaches, dynamic dissipation in CMOS, effects of V_{DD} & V_T on speed, constraints on V_T reduction, transistor sizing & optimal gate oxide thickness, impact of technology scaling, technology innovations.

UNIT – 2 Low Power Circuit Techniques

Power consumption in circuits, flip-flops & latches, high capacitance nodes, energy recovery, reversible pipelines, high performance approaches.

UNIT – 3 Low Power Clock Distribution

Power dissipation in clock distribution, single driver Versus distributed buffers, buffers & device sizing under process variations, zero skew Vs Tolerable skew, chip & package co-design of clock network.

UNIT – 4 Logic Synthesis for Low Power estimation techniques

Power minimization techniques, Low power arithmetic components- circuit design styles, adders, multipliers.

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UNIT – 5 Low Power Memory Design

Sources & Reduction of power dissipation in memory subsystem, sources of power dissipation in DRAM & SRAM, low power DRAM circuits, low power SRAM circuits.

Low Power Microprocessor Design System: Power management support, architectural trade-offs for power, choosing the supply voltage, low-power clocking, implementation problem for low power.

Text Books:

1. P. Rashinkar, Paterson and L. Singh, “Low Power Design Methodologies”, Kluwer Academic,2002.
2. Kaushik Roy, Sharat Prasad, “Low power CMOS VLSI circuit design”, John Wiley sonsInc.,2000.

Reference Books:

1. J.B.Kulo and J.H Lou, “Low voltage CMOS VLSI Circuits”, Wiley, 1999.
2. A.P.Chandrasekaran and R.W.Broadersen, “Low power digital CMOS design”,Kluwer,1995.
3. Gary Yeap, “Practical low power digital VLSI design”, Kluwer, 1998.

CO-PO Mapping:

1: Slight (Low) 2: Moderate (Medium) 3: Substantial (High) '-': No Correlation

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	2	1	3							1		
CO2	2	2	-							3		
CO3	2	-	3							1		
CO4	2	2	-							1		
CO5	3	-	-							2		

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M.Tech - VLSI & Embedded Systems Course Structure and Syllabus: (2020-21)

Regulation GRBT-19	Godavari Institute of Engineering & Technology (Autonomous)	I M.Tech. II Sem (2 nd Semester)			
CourseCode	ANALOG AND DIGITAL CMOS VLSI DESIGN LAB				
Teaching	Total Contact Hours- 30	L	T	P	C
Prerequisites: VLSI Design Technology and Analog/Digital IC Design.		0	0	4	2

Course Objectives:

1. Understand the basic concepts of VLSI devices.
2. Learn the basic design and structure of Amplifiers
3. Learn the basic structure and logics of Logic Gates.
4. Design of Latches and Flip-Flops.

Course Outcomes:

On Completion of the course, students will be able to	
CO1:	Design basic concepts of VLSI devices and Amplifiers
CO2:	Design the Cascade and simple current mirrors
CO3:	Design the Logic gates using the software tools and verifying them
CO4:	Design Flip-Flops, Latches and counters

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List of Experiments:

1. MOS Device Characterization and parametric analysis
2. Common Source Amplifier
3. Common Source Amplifier with source degeneration
4. Cascode amplifier
5. Simple current mirror
6. Cascode current mirror.
7. Wilson current mirror.
8. Full Adder
9. RS-Latch
10. Clock Divider
11. JK-Flip Flop
12. Synchronous Counter
13. Asynchronous Counter
14. Static RAM Cell

CO-PO Mapping:

1: Slight (Low) 2: Moderate (Medium) 3: Substantial (High) '-': No Correlation

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	2	2	3	-	3	-	3	3	-	-	3
CO2	3	2	2	3	2	3	2	3	3	-	-	3
CO3	3	2	2	3	2	3	2	3	3	2	2	3
CO4	3	2	2	3	2	3	2	3	3	2	2	3

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Regulation GRBT-19	Godavari Institute of Engineering & Technology (Autonomous)	I M.Tech. II Sem (2 nd Semester)			
CourseCode	REAL TIME OPERATING SYSTEMS LAB				
Teaching	Total Contact Hours- 30	L	T	P	C
Prerequisites: VLSI Design Technology and Analog/Digital IC Design.		0	0	4	2

Course Objectives:

1. To learn the basic designs using an RTOS.
2. To know the functions and types of RTOS for embedded systems.
3. To analyze the issues in real time operating systems.
4. To understand the programming concepts of RTOS.
5. To analyze the operating system software.

Course Outcomes:

On Completion of the course, the students will be able to	
CO1:	Illustrate real time programming concepts.
CO2:	Apply RTOS functions to implement embedded applications.
CO3:	Understand Interrupt service mechanism and I/O subsystem design.
CO4:	Describe various types of Memory Management of RTOS.
CO5:	Understand fundamentals of design consideration for embedded applications.

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The students are required to perform at least SIX experiments from Part-I and TWO experiments from Part-II.

List of Experiments:**Part-I: Experiments using ARM-926 with PERFECT RTOS**

1. Register a new command in CLI.
2. Create a new Task.
3. Interrupt handling.
4. Allocate resource using semaphores.
5. Share resource using MUTEX.
6. Avoid deadlock using BANKER'S algorithm.
7. Synchronize two identical threads using MONITOR.
8. Reader's Write's Problem for concurrent Tasks.

Part-II: Experiments on ARM-CORTEX processor using any open source RTOS(Coo-Cox-Software-Platform)

1. Implement the interfacing of display with the ARM- CORTEX processor.
2. Interface ADC and DAC ports with the Input and Output sensitive devices.
3. Simulate the temperature DATA Logger with the SERIAL communication with PC.
4. Implement the developer board as a modem for data communication using serial port communication between two PC's.

Lab Requirements:**Software:**

- Eclipse IDE for C and C++ (YAGARTO Eclipse IDE), Perfect RTOS Library, COO-COX Software Platform, YAGARTO TOOLS, and TFTP SERVER.
- LINUX Environment for the compilation using Eclipse IDE & Java with latest version.

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Hardware:

- The development kits of ARM-926 Developer Kits and ARM-Cortex Boards.

CO-PO Mapping:
1: Slight (Low) 2: Moderate (Medium) 3: Substantial (High) '-' : No Correlation

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	2	1	3	-	1	1	1	-	-	-	1	3
CO2	2	1	1	-	-	-	1	2	-	2	-	-
CO3	2	-	3	2	1	2	2	-	3	-	2	-
CO4	1	2	-	-	-	2	3	3	2	1	-	3
CO5	3	-	-	2	-	1	-	2	-	2	-	-

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II YEAR I SEMESTER

Regulation GRMT-20	Godavari Institute of Engineering & Technology (Autonomous)	II M.Tech. I Sem (3 rd Semester)			
CourseCode	INTERNET OF THINGS AND APPLICATIONS (Professional Elective – V)				
Teaching	Total contact hours-45	L	T	P	C
Prerequisites: Knowledge of Logic Gates, Computer Networks, Sensors, Microprocessors, Microcontrollers, Serial & Parallel Communication.		3	-	-	3

Course Objectives:

1. To understand the basic concepts of Internet of things.
2. To develop understanding with layered Wired and Wireless protocols.
3. To develop understanding with Arduino board, Raspberry pi board and Arduino IDE.
4. To develop understanding with Data analytics and supporting services.
5. To develop understanding with Big data services and Sensors.

Course Outcomes:
On Completion of the course, the students will be able to

CO1:	Apply the Knowledge in IOT Technologies and Data management.
CO2:	Determine the values chains Perspective of M2M to IOT.
CO3:	Implement the state of the Architecture of an IOT.
CO4:	Compare IOT Applications in Industrial & real world.
CO5:	Demonstrate knowledge and understanding the security and ethical issues of an IOT.



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UNIT – 1 Fundamentals of IoT

Evolution of Internet of Things, Enabling Technologies, IoT Architectures, oneM2M, IoT World Forum (IoTWF) and Alternative IoT models, Simplified IoT Architecture and Core IoT Functional Stack, Fog, Edge and Cloud in IoT, Functional blocks of an IoT ecosystem, Sensors, Actuators, Smart Objects and Connecting Smart Objects. IoT Platform overview: Overview of IoT supported Hardware platforms such as: Raspberry pi, ARM Cortex Processors, Arduino and Intel Galileo boards.

UNIT – 2 IoT Protocols

IT Access Technologies: Physical and MAC layers, Topology and Security of IEEE 802.15.4, 802.15.4g, 802.15.4e, 1901.2a, 802.11ah and Lora WAN, Network Layer: IP versions, Constrained Nodes and Constrained Networks, Optimizing IP for IoT: From 6LoWPAN to 6Lo, Routing over Low Power and Lossy Networks, Application Transport Methods: Supervisory Control and Data Acquisition, Application Layer Protocols: CoAP and MQTT.

UNIT – 3 Design and Development

Design Methodology, Embedded computing logic, Microcontroller, System on Chips, IoT system building blocks, Arduino, Board details, IDE programming, Raspberry Pi, Interfaces and Raspberry Pi with Python Programming.

UNIT – 4 Data Analytics and Supporting Services

Structured Vs Unstructured Data and Data in Motion Vs Data in Rest, Role of Machine Learning — No SQL Databases, Hadoop Ecosystem, Apache Kafka, Apache Spark, Edge Streaming Analytics and Network Analytics, Xively Cloud for IoT, Python Web Application Framework, Django, AWS for IoT, System Management with NETCONF-YANG.

UNIT – 5 Case Studies/Industrial Applications

IoT applications in home, Infrastructures, Buildings, Security, Industries, Home appliances, other IoT electronic equipment. Use of Big Data and Visualization in IoT, Industry 4.0 concepts. Sensors and sensor Node and interfacing using any Embedded target boards (Raspberry Pi / Intel Galileo/ARM Cortex/ Arduino).

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Text Books:

1. IoT Fundamentals: Networking Technologies, Protocols and Use Cases for Internet of Things, David Hanes, Gonzalo Salgueiro, Patrick Grossetete, Rob Barton and Jerome Henry, Cisco Press, 2017.
2. Internet of Things – A hands-on approach, Arshdeep Bahga, Vijay Madisetti, Universities Press, 2015.
3. The Internet of Things – Key applications and Protocols, Olivier Hersent, David Boswarthick, Omar Elloumi and Wiley, 2012 (for Unit 2).

Reference Books:

1. From Machine-to-Machine to the Internet of Things: Introduction to a New Age of Intelligence - Jan Holler, Vlasios Tsiatsis, Catherine Mulligan, Stefan Avesand, Stamatis Karnouskos, David Boyle, 1st Edition, Academic Press, 2014.
2. Architecting the Internet of Things, Dieter Uckelmann, Mark Harrison, Michahelles and Florian (Eds), Springer, 2011.
3. Recipes to Begin, Expand, and Enhance Your Projects - Michael Margolis, Arduino Cookbook and O'Reilly Media, 2nd Edition 2011.

Web Links:

1. <https://thingspeak.com>
2. <https://www.blynk.cc/getting-started>
3. <http://www.arduino.cc>
4. <https://coap.technology>

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CO-PO Mapping:
1: Slight (Low) 2: Moderate (Medium) 3: Substantial (High) '-' : No Correlation

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	2	1	3	-	1	1	1	-	-	-	1	3
CO2	2	1	1	-	-	-	1	2	-	2	-	-
CO3	2	-	3	2	1	2	2	-	3	-	2	-
CO4	1	2	-	-	-	2	3	3	2	1	-	3
CO5	3	-	-	2	-	1	-	2	-	2	-	-

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Regulation GRMT-20	Godavari Institute of Engineering & Technology (Autonomous)	II M.Tech. I Sem (3 rd Semester)			
Course Code	DESIGN FOR TESTABILITY (Professional Elective – V)				
Teaching	Total contact hours - 50	L	T	P	C
Prerequisites: Switching Theory for Logic Design, VLSI Design, Digital IC Design		3	-	-	3

Course Objectives:

1. To learn various types of faults and fault modelling.
2. To comprehend the need for testing and testable design of digital circuits
3. To illustrate methods and algorithms for testing digital combinatorial networks and test pattern generation
4. To exemplify methods for testing sequential circuits and memory testing
5. To infer testing methods using Boundary scan, Built-in self test and other advanced topics in digital circuit design.

Course Outcomes:

On Completion of the course, the students will be able to	
CO1:	Analyze the need for fault modeling and testing of digital circuits
CO2:	Generate fault lists for digital circuits and compress the tests for efficiency
CO3:	Create tests for digital memories and analyze failures in them
CO4:	Apply boundary scan technique to validate the performance of digital circuits
CO5:	Design built-in self tests for complex digital circuits

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UNIT – 1 Faults in Digital Circuits

Failures and Faults, Modeling of faults, Temporary Faults. Logic Simulation: Applications, Problems in simulation-based design verification, types of simulation, The unknown logic values, compiled simulation, event-driven simulation, Delay models, Element evaluation, Hazard detection, Gate-level event-driven Simulation.

UNIT – 2 Test Generation for Combinational Logic Circuits

Fault Diagnosis of digital circuits, Test generation techniques for combinational circuits, Detection of multiple faults in Combinational logic circuits. Testable Combinational logic circuit design: The Read-Muller expansion technique, Three level OR-AND-OR design, Automatic synthesis of testable logic.

UNIT – 3 Testable Combinational Logic Circuit Design

Testable design of multilevel combinational circuits, Synthesis of random pattern testable combinational circuits, Path delay fault testable combinational logic design, Testable PLA design. Test generation for Sequential circuits: Testing of sequential circuits as Iterative combinational circuits, state table verification, Test generation based on Circuit Structure, Functional Fault models, test Generation based on Functional Fault models.

UNIT – 4 Design of Testable Sequential Circuits

Controllability and observability, Ad-Hoc design rules for improving testability, Design of diagnosable sequential circuits, The scan-path technique for testable sequential circuit design, Level Sensitive Scan Design (LSSD), Random Access Scan Technique, Partial scan, Testable sequential circuit design using Nonscan Techniques, Cross check, Boundary Scan.

UNIT – 5 Built-In Self-Test

Test pattern generation for BIST, Output response analysis, Circular BIST, BIST Architectures. Testable Memory Design: RAM Fault Models, Test algorithms for RAMs, Detection of pattern-sensitive faults, BIST techniques for RAM chips, Test generation and BIST for embedded RAMs.

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Text Books:

1. Lala Parag K., Digital Circuit Testing and Testability, New York, Academic Press, 1997.
2. Abramovici M, Breuer M A and Friedman A D, Digital Systems Testing and Testable Design, Wiley, 1994.

Reference Books:

1. Vishwani D Agarwal, Essential of Electronic Testing for Digital, Memory and Mixed Signal Circuits, Springer, 2002.
2. Wang, Wu and Wen, VLSI Test Principles and Architectures, Morgan Kaufmann, 2006.
3. Douglas A Pucknell & Kamran Eshragian, Basic VLSI Design, PHI 3rd Edition (Original Edition – 1994).

CO-PO Mapping:
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	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	1	2	2	2	1			2				1
CO2	1	3	1	2	2		1	2				
CO3	2	2	1	2	2		1	2				2
CO4	1	1	1	1	2	2	1	3				
CO5	1	1	1	2	2	2		3				2

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Regulation GRMT-20	Godavari Institute of Engineering & Technology (Autonomous)	II M.Tech. I Sem (3 rd Semester)			
CourseCode	ARTIFICIAL INTELLIGENCE (Professional Elective – V)				
Teaching	Totalcontacthours-45	L	T	P	C
Prerequisites: Knowledge of Discrete Mathematics, Algorithms and Programming.		3	-	-	3

Course Objectives:

1. To gain a historical perspective of AI and its foundations.
2. To become familiar with basic principles of AI toward problem solving, inference, perception, knowledge representation and learning.
3. To understand mathematical models and apply them to a range of AI problems.
4. To experiment with a machine learning model for simulation and analysis.
5. To investigate applications of AI techniques in artificial neural networks and other machine learning models.

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On completion of the course, the students will be able to	
CO1:	Demonstrate fundamental understanding of the history of artificial intelligence (AI) and its foundations.
CO2:	Apply basic principles of AI in solutions that require problem solving, inference, perception, knowledge representation and learning.
CO3:	Understand mathematical models and apply them to a range of AI problems.
CO4:	Experiment with a machine learning model for simulation and analysis.
CO5:	Investigate applications of AI techniques in artificial neural networks and other machine learning models.

UNIT – 1 Introduction to AI

What is AI (Artificial Intelligence), The AI problems, The underlying assumption, What are AI techniques, The level of the model, Criteria for success, some general references, one final word problems. State space search & Heuristic search techniques: Defining the problem as a state space search, Production system, Production system characteristics and Issues in the design of search programs, Additional problems. Generate-and-test, Hill climbing, Best-first search, Problem reduction, Constraint satisfaction, Means-ends analysis.

UNIT – 2 Knowledge Representation Issues

Representations and mappings, Approaches to knowledge representation. Representing knowledge using predicate logic: Representation of simple facts in logic, Representing instance and isa relationships, Computable functions and predicates, Resolution. Representing knowledge using rules: Procedural versus Declarative knowledge, Logic programming, Forward versus Backward reasoning.

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UNIT – 3 Symbolic Reasoning Under Uncertainty

Introduction to Non-monotonic Reasoning, Logics for Non-monotonic reasoning. Statistical reasoning: Probability and Bayes' Theorem, Certainty factors and rule-base systems, Bayesian networks, Dempster Shafer Theory, Fuzzy Logic. Weak Slot-and-Filler Structures: Semantic Nets, Frames. Strong Slot-and-Filler Structures: Conceptual Dependency, Scripts, CYC.

UNIT – 4 Design Specification and Verification

Game Playing: Overview and Example Domain: Overview, Minimax, Alpha-Beta Cut-off, Refinements, Iterative deepening, The Blocks World, Components of a Planning System, Goal Stack Planning, Nonlinear Planning using Constraint Posting, Hierarchical Planning, Reactive Systems, Other Planning Techniques. Understanding: What is understanding? What makes it hard? As constraint satisfaction.

UNIT – 5 Natural Language Processing

Introduction, Syntactic Processing, Semantic Analysis, Syntactic Analysis, Discourse and Pragmatic Processing, Spell Checking Connectionist Models: Introduction, Hopfield Network, Learning In Neural Network, Application of Neural Networks, Recurrent Networks, Distributed Representations, Connectionist AI And Symbolic AI.

Text Books:

1. Artificial Intelligence, Elaine Rich and Kevin Knight, 2nd Edition, Tata McGraw Hill, 2005.
2. Artificial Intelligence: A Modern Approach, Stuart Russel and Peter Norvig, 3rd Edition, Prentice Hall, 2009.

Reference Books:

1. "Artificial Intelligence: A Modern Approach" by Stuart Russell and Peter Norvig.
2. "Artificial Intelligence: A New Synthesis" by Nils J Nilsson.
3. "Artificial intelligence, structures, and Strategies for Complex problem solving" -George F Luger, 5th ed, PEA.

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	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	1	2	2	2	1	-	-	2	-	-	-	1
CO2	1	3	1	2	2	-	1	2	-	-	-	
CO3	2	2	1	2	2	-	1	2	-	-	-	2
CO4	1	1	1	1	2	2	1	3	-	-	-	
CO5	1	1	1	2	2	2	-	3	-	-	-	2